

ABSTRACT

A processor includes a cache memory with a data storage unit operating at a first clock frequency, and a tag unit and hit/miss logic operating at a second clock frequency different than the first clock frequency. The data storage unit may advantageously be clocked faster than the tag unit and hit/miss logic, such as two times (2X) faster. The processor may also include a replay mechanism for recovering from data speculation when the hit/miss logic or the tag unit signals that speculated data from the higher clocked data storage unit is, in fact, invalid.